This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Previously Presented) A printed circuit board having an EMI shielding structure for shielding wiring circuit traces on a plurality of circuit trace layers applied on a plurality of printed circuit board layers and electrically isolated there between by the printed circuit board layers and having a printed circuit board multi- layer structure, characterized by:

a trench having a rim about an opening of the trench at a top printed circuit board layer and said trench extending through a plurality of printed circuit board layers to a grounding plane exposing said grounding plane and said trench having an interior wall with a conductive plating material applied over said interior wall and said trench having a length greater than two times a breadth of said trench and wherein the trench completely surrounds an area of the printed circuit board and wherein said conductive plating material electrically connects to said exposed grounding plane.

3-8 (Cancelled)

9. (Previously Presented) A printed circuit board having a reference plane structure for fixing a potential reference for a plurality of wiring circuit trace layers that are electrically isolated there between by a plurality of printed circuit board layers and having a printed circuit board layer with a main surface, characterized by:

a wire trace circuit layer applied to said main surface;

a printed circuit board-insulation layer formed over said wire trace circuit layer;

a reference plane applied over the printed circuit board insulation layer;

a trench having an interior wall extending through and exposing the wire trace circuit layer, and the trench further extending through the insulation layer to the reference plane wherein the reference plane is exposed and wherein the trench completely surrounds an area of the printed circuit board; and

a conductive plating layer on the interior wall electrically connects the wire trace circuit layer to the reference plane.

10. (Previously Presented) The printed circuit board of claim 9, wherein the trench completely encompasses the wire trace circuit layer.

11. (Previously Presented) The printed circuit board of claim 9, wherein the reference plane is fixed at a ground potential.

12. (Previously Presented) The printed circuit board of claim 9, wherein the reference plane is fixed at a reference voltage.

13-16 (Cancelled)

17. (Withdrawn) A method of interconnecting a plurality of wire traces applied on a plurality of printed circuit board layers characterized by the steps of:

applying a first wire trace to a main surface of a first printed circuit board layer wherein said first wire trace has a first terminal landing pad;

forming an insulation layer over said first wire trace;

applying a second wire trace over the insulation layer, said second wire trace having a second terminal landing pad vertically aligned over the first terminal landing pad;

cutting through the first terminal landing pad, the insulation layer, and the second terminal landing pad; and

plating the interior wall of the hole with an electrically conductive material thereby electrically connecting the first wire trace and

second wire trace by the connection established between the first terminal landing pad and second terminal landing pad.

18. (Withdrawn) The method of interconnecting a plurality of wire traces of claim 17 wherein in the cutting step, the cutting is by plasma ablation.

19. (Withdrawn) The method of interconnecting a plurality of wire traces of claim 17 wherein in the cutting step, the cutting is by laser processing.

20. (Withdrawn) A method of grounding and shielding a plurality of wire traces applied on a plurality of printed circuit board layers characterized by the steps of:

applying a wire trace to a main surface of a printed circuit board layer;

forming an insulation layer over said wire trace;

applying a grounding plane over the insulation layer;

cutting through the printed circuit board layer and the insulation layer to the grounding plane thereby forming a trench at least partially about the wire trace, the trench having an interior wall exposing the wire trace and the grounding plane; and

plating the interior wall of the trench with an electrically conductive material thereby connecting the wire trace to the grounding plane.

21. (Previously Presented) A printed circuit board having an EMI shielding structure for shielding a plurality of wire trace layers, characterized by:

a printed circuit board layer having a wire trace applied thereto;

an insulation layer; and

a grounding plane;

a first trench having an interior wall and forming a perimeter completely surrounding the wire trace and extending through the printed circuit board layer and extending to the ground plane and exposing said ground plane; and

an electrically conductive plating material applied upon the interior wall of the first trench and electrically connecting to the exposed ground plane providing a perimeter shield for the trace.

22. (Cancelled)

23. (Previously presented) The printed circuit board of claim 21, further characterized by:

a second trench having an interior wall and spaced a distance from the first trench such that the wire trace extends between the first trench and second trench, the second trench extending through the printed circuit board layer and extending to the ground plane exposing said ground plane,

wherein the interior wall of the second trench is plated with an electrically conductive plating material electrically connecting to the exposed ground plane thereby providing a double trench shield.

24. (Previously presented) The printed circuit board of claim 21, further characterized by:

an EMC sensitive track of conductive material extending wholly within a perimeter defined by the first trench and disposed between a plurality of circuit board insulation layers through which the first trench extends.

25. (Previously presented) A printed circuit board having an EMI shielding structure for shielding a plurality of wire trace layers, characterized by:

a plurality of printed circuit board layers having a plurality of wire trace layers, each printed circuit board layer separated by an insulation layer and having a grounding plane layer;

a first trench extending from a top printed circuit board layer to the grounding plane layer and the first trench having;

an electrically conductive plating applied over an interior wall of the first trench and electrically connecting to the ground plane; and wherein

the first trench completely surrounds at least an area of the printed circuit board layers.

26. (Previously presented) The printed circuit board of claim 25, further characterized by:

a second trench disposed interior to the first trench and said second trench extending substantially in parallel to the first trench;

and the second trench having an electrically conductive plating applied over an interior wall thereof electrically connecting to the ground plane and an EMC sensitive track extending in a printed circuit board layer positioned between the first trench and the second trench.

27. (Cancelled)

28. (Cancelled)

29. (Withdrawn) The method of claim 17 wherein the non-circular shaped cross section of the through hole is a cross, a "U", an "L", an "E", a square or rectangle, a "double cross", a star, an oval, a continuous curve, or an irregular shape.

30. (Previously Presented) A printed circuit board having an EMI shielding structure for shielding a plurality of wire trace layers, characterized by:

a plurality of printed circuit board layers having a plurality of wire trace layers, each printed circuit board layer separated by an insulation layer and having a grounding plane layer;

a first trench extending from a top printed circuit board layer to the grounding plane layer and the first trench having an electrically conductive plating applied over an interior wall of the first trench and electrically connecting to the ground plane and wherein the first trench completely surrounds an area of the printed circuit board; and

a second trench disposed interior to the first trench and said second trench extending substantially in parallel to the first trench and the second trench having an electrically conductive plating applied over an interior wall thereof electrically connecting to the ground plane; and

at least two EMC sensitive tracks extending in a printed circuit board layer positioned between the first trench and the second trench.